

How Design Automation Is Reshaping the Foundry-Client Dynamic

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Foundries may soon have a lot to say about the choices designers make in the way they prepare test patterns. Imagine the following scenario: As parts go through production testing, data is collected from every failing die and stored in a huge database, along with detailed information about the fabrication process, the physical design, and defect phenomena. Software analyzes the data and determines the likely cause of each failure. The analysis results are combined with process and device simulators and transformed into subtle adjustments for wafer processing. The constant tweaking of manufacturing parameters leads to steady improvement in manufacturing yield. Realizing higher yield faster gives foundries their competitive advantage.

The imagined scenario is taking shape at foundries and integrated device manufacturers today. To achieve this capability, called volume diagnostics, wafer manufacturers are relying on automatic test pattern generation (ATPG) diagnostics tools such as Synopsys' TetraMAX® to automate the process of accurately identifying logic in fabricated parts that could contribute to observed mismatches in the expected responses. Moreover, some of these tools now have extensions that allow them to pass failure information to yield management solutions (YMS) that perform complex data mining and cross-correlation of defect, fabrication, and physical design data across multiple wafers and lots. State-of-the-art YMS and Technology Computer-Aided Design (TCAD)-for-manufacturing systems such as Synopsys' Odyssey™ YMS and Sentaurus solutions can identify the underlying physical failure mechanisms and take corrective actions to steadily improve yield.

Thanks to these tool innovations, volume diagnostics is gathering critical mass in fabs and has the potential to transform the relationship between the foundry and its fabless clientele. On the one hand, the foundry benefits by achieving higher intrinsic manufacturing yield. For this to happen, its customers must embed sufficient DFT infrastructure in production ICs to ensure accurate failure diagnostics. They must also transfer to the foundry enough information about a product's physical design to ensure accurate characterization of systematic defects caused by complex interactions between the layout and wafer processing. On the other hand, the foundry's fabless clientele benefit from gaining earlier access to higher yields. And when the foundry returns relevant parametric data to a client, designers can then perform their own ATPG failure diagnostics for a given product—both to validate the foundry's promised yield and to determine how to make incremental design modifications to further improve yield for that product.

Interestingly, the success of volume diagnostics depends on a very recent innovation in ATPG diagnostics tools: the ability to accurately diagnose failures for designs implemented with scan compression, a technique used on-chip to reduce the amount of data needed for digital testing. Until recently, accurate diagnostics was possible only for ATPG patterns that utilized standard scan DFT structures. This meant that if designers had implemented scan compression to take advantage of cost savings from test time reduction, failing parts would have to be reconfigured in standard scan mode and the responses scanned out uncompressed. This was not cost-effective

and so diagnostics remained an off-line activity, outside the production loop. To meet the high-throughput requirements of volume diagnostics, ATPG diagnostics tools had to be enhanced so they could trace faults backward through many possible logic cones to isolate the sources of pattern mismatches. Only then could they co-exist with scan-compressed designs.

Still, there are practical limits to the expected accuracy of scan-compressed diagnostics: if you keep increasing the amount of compression, you gradually lose diagnostics resolution. Although a tool's compression parameters can influence the outcome, typically the more data compression implemented on-chip, the lower the confidence in isolating fault candidates across a spectrum of fault models. And this brings us back to my opening statement about the choices designers make in preparing test patterns. Designers should evaluate the amount of compression added to their designs, not just in terms of its affect on the total costs of test, but also its impact on the accuracy of diagnostics and the potential for improving product yield. While innovations in design and process automation are creating opportunities for both foundries and their fabless clientele to create sustainable competitive advantage, I anticipate foundries will have increasing influence on decisions their customers make regarding tools and methodologies that facilitate volume diagnostics. In the meantime, designers implementing scan compression need to be aware of the stakes involved.